EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	298	380/29.ccls. and @ad<"20010126"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:21
L2	78	713/192.ccls. and @ad<"20010126"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:38
L3	851.	380/28.CCLS. AND @ad<"20010126"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT;	OR	ON	2007/10/18 14:21
L4	1129	(L1 or L2 or L3)	US-PGPUB; US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:21
L5	537	DES and bit and ("XOR" or exclusive) and (key\$3 with dependent\$3) and encrypt\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:22
L6	261	L5 and (register and (circuit or IC or hardware or micro or microprocessor or chip or DMA or DSP or prom or eprom or card or smartcard) and wir\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:24
L7 .	13	L6 and L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT;	OR	ON	2007/10/18 14:25
L8	85	L6 and @ad<"20010126"	IBM_TDB US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:25

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L9	45	("713"/\$.ccls. or "380"/\$.ccls.) and L8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:37
L10	63	(DES with FPGA) and (single with chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:38
L11	17	L10 and @ad<"20010126"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:45
L12	12	L11 and encrypt\$3 and key\$3	US-PGPUB; USPAT; USOCR;	OR	ON	2007/10/18 14:42
			EPO; JPO; DERWENT; IBM_TDB			
L13	4364	(hardware or circuit or FPGA or micro or microprocessor or chip or IC or circuit or prom or eprom) with DES with (fast\$3 or highspeed or (high\$3 near3 speed\$3) or quick\$3 or rapid\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:44
L14	5007	(hardware or circuit or FPGA or micro or microprocessor or chip or IC or circuit or prom or eprom) with DES with (efficient\$3 or fast\$3 or highspeed or (high\$3 near3 speed\$3) or quick\$3 or rapid\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:45
L15	120	L14 and encrypt\$3 and key\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:45
L16	50	L15 and @ad<"20010126"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/18 14:46



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Fernandez, I.B.; Subbarao, W.V.;

Southeastcon '94. 'Creative Technology Transfer - A Global Affair'., Proceedings of the 1994

IEEE

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Digital Object Identifier 10.1109/SECON.1994.324268

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2. High performance DES encryption in VirtexTM FPGAs using JBitsTM

Patterson, C.;

Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on

17-19 April 2000 Page(s):113 - 121

Digital Object Identifier 10.1109/FPGA.2000.903398

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A single-chip FPGA implementation of the data encryption standard (DES) algorithm

Wong, K.; Wark, M.; Dawson, E.;

Global Telecommunications Conference, 1998. GLOBECOM 98. The Bridge to Global

Integration, IEEE

Volume 2, 8-12 Nov. 1998 Page(s):827 - 832 vol.2

Digital Object Identifier 10.1109/GLOCOM.1998.776849

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4. A flip-chip implementation of the Data Encryption Standard (DES)

Schaffer, T.; Glaser, A.; Rao, S.; Franzon, P.;

Multi-Chip Module Conference, 1997. MCMC '97., 1997 IEEE

4-5 Feb. 1997 Page(s):13 - 17

Digital Object Identifier 10.1109/MCMC.1997.569339

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5. A high level language implementation of the data encryption standard and a bit-slice

Sixel, R.G.; Monteiro, R.S.; Anido, M.L.;

Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on

Volume 1, 8-11 Aug. 2000 Page(s):266 - 269 vol.1

Digital Object Identifier 10.1109/MWSCAS.2000.951635

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 Advanced VLSI validated input security device employing data and hardward features Iliev, V.; Dlay, S.S.; McLauchlan, M.R.; Koelmans, A.M.; Kinniment, D.J.; Computers and Digital Techniques, IEE Proceedings-Volume 136, Issue 6, Nov 1989 Page(s):471 - 477 AbstractPlus Full Text: PDF(668 KB) IET JNL 	validation
7. Security Requirements and Protocols for a Broadcast Scenario Kent, S.; Communications, IEEE Transactions on [legacy, pre - 1988] Volume 29, Issue 6, Jun 1981 Page(s):778 - 786 AbstractPlus Full Text: PDF(1168 KB) IEEE JNL Rights and Permissions	
 VLSI implementation of an OFB processor for encryption of real-time data Young-Chul Kim; Kwang-Ok Kim; Tae-Won Lee; ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Confe 28-30 Aug. 2000 Page(s):179 - 182 Digital Object Identifier 10.1109/APASIC.2000.896938 <u>AbstractPlus</u> Full Text: PDF(292 KB) IEEE CNF Rights and Permissions 	rence on

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Volume 2, Issue 6, Dec 1984 Page(s):901 - 909

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2. A Very High Reliability Fast Bipolar IC Technology for Use in Undersea Optical Fiber

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Fourrier, J.; Pestie, J.;

Selected Areas in Communications, IEEE Journal on

Volume 2, <u>Issue 6</u>, Nov 1984 Page(s):941 - 949

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3. Advanced VLSI validated input security device employing data and hardware validation T

Iliev, V.; Dlay, S.S.; McLauchlan, M.R.; Koelmans, A.M.; Kinniment, D.J.;

Computers and Digital Techniques, IEE Proceedings-

Volume 136, <u>Issue 6</u>, Nov 1989 Page(s):471 - 477

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4. All-optical switching and XOR-gating using cross-polarization modulation in a semiconductor optical amplifier

Erasme, D.; Soto, H.; Guekos, G.;

Lasers and Electro-Optics Europe, 2000. Conference Digest. 2000 Conference on

10-15 Sept 2000 Page(s):1 pp.

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